IN THE SPECIFICATION:

Please amend paragraph number **[0003]** as follows:

[0003] Variation in clock signal arrival time is referred to as clock skew. A variety of techniques have been used to provide clock connections that are symmetrical and all of the same length in order to minimize clock skew at the various logic elements, including, for example, the methods of Yip and Carrig. *See*, K. Yip, "Clock tree distribution: balance is essential for ~~a deep submicron~~ deep-submicron ASIC design to flourish," IEEE Potentials, vol. 16, no. 2, pp. 11-14, Apr-May 1997; and K.M. Carrig et al., "Clock methodology for high-performance microprocessors," Proc. Custom Integrated Circuits Conference, Santa Clara, CA, May 5-8, pp. 119-122, 1997. A number of prior art approaches are illustrated in FIGS. 1A - 1D.

Please amend paragraph number **[0010]** as follows:

[0010] There remains a need for a method of coordinating the timing of clock and data signals on a chip that can be achieved with a simple design and minimum number of critical paths on the chip. It would be desirable to reduce the power consumption associated with ~~clock distribution~~ clock-distribution lines or other chip timing circuitry. It would also be desirable to reduce the sensitivity of chip timing to process variations and various intermittent noises. Finally, there is an ongoing need for the development of higher speed methods for clocking data to provide enhanced chip performance.

Please amend paragraph number **[0028]** as follows:

[0028] FIG. 3 is a block diagram of a device 2 including circuitry for performing phase shift keying of clock and digital data signals and subsequent demodulation of the PSK signals to retrieve the clock and digital data signals. Device 2 may be an integrated circuit, interposer, circuit board, or similar device. Device 2 includes phase shift keying circuitry 4, which performs phase shift keying of the digital data signal X onto the clock signal CLK to generated phase shift keyed signals V_X and $V_{\bar{X}}$. Phase shift keying circuitry 4 is located near the clock source on device 2. PSK signals V_X and $V_{\bar{X}}$ are transmitted on interconnection lines 9 and 13 to digital

signal demodulator 6. Digital signal demodulator 6 demodulates PSK signals V_x and $V_{\bar{x}}$ to retrieve digital data signal X. Digital data signal X and PSK signals V_x and $V_{\bar{x}}$ are input to clock signal demodulator 8, which demodulates PSK signals V_x and $V_{\bar{x}}$ to retrieve the clock signal. The clock signal and digital data signal X are input to clocked element 10 with no relative time delay between the two. Digital signal demodulator 6 and clock signal demodulator 8 are located close to clocked element 10 but may be located at some distance from phase shift keying circuitry 4.

Please amend paragraph number **[0029]** as follows:

[0029] Fig. 4 is a schematic diagram of differential phase shift keying circuitry 4 that may be used to perform the differential phase shift keying signal interconnection technique of the present invention. A sinusoidal oscillator signal sin(ωt) having a radian frequency ω at the clock signal frequency for the chip is generated by oscillator 1. The oscillator signal is sent simultaneously to phase shifter 3 and phase shifter 5. Digital signal X is input to phase shifter 3 and controls the phase shift produced in the oscillator signal by phase shifter 3, while the complementary digital signal ~~$\bar{x}$ is~~ $\bar{X}$ is input to and controls the phase shift produced in the oscillator signal by phase shifter 5. The output of phase shifter 3 is fed to driver amplifier 7 and, from there, transmitted on interconnection line 9. The output of phase shifter 5 is fed to driver amplifier 11 and subsequently transmitted on interconnection line 13. Interconnection line 9 and interconnection line 13 are low impedance interconnection lines with matched terminating impedances 15 and 17, respectively.

Please amend paragraph number **[0031]** as follows:

[0031] FIG. 6 depicts phase shifter 5, which is a lag phase shift network made up of voltage variable resistor 23 and capacitor 25 forming a low pass filter. Capacitor 25 has a capacitance C2 and voltage variable resistor 23 has a resistance of R2. Voltage variable resistor 23 is an NMOS transistor configured as a voltage variable resistor, with complementary

digital ~~input $\bar{x}$~~ input $\overline{X}$ connected to its gate to regulate the value of resistance R2. Phase shifter 5 produces a phase shift of equal magnitude but opposite sign to that produced by phase shifter 3; ~~thus~~ thus, it produces a negative phase shift φ in the input signal. Thus, when the input to phase shifter 5 is $\sin(\omega t)$ ~~and $\bar{x}$~~ and $\overline{X}$ has a logical high value, the output will be $V_{\bar{x}} = A\sin(\omega t - \varphi$ and ~~when $\bar{x}$~~ when $\overline{X}$ has a logical low value, the output will be $V_{\bar{x}} = A\sin(\omega t)$ where A is the arbitrary constant found in the expression for V_x. $V_{\bar{x}}$ is plotted in FIG. 7B.

Please amend paragraph number **[0033]** as follows:

[0033] The phase shift keyed signals V_x and $V_{\bar{x}}$ are transmitted on matched interconnection lines 9 and 13 to the vicinity of the clocked element 10. V_x and $V_{\bar{x}}$ each contain both clock and phase shift keyed digital data. Any signal skew which occurs over the length of interconnection lines 9 and 13 should be substantially the same for the signals on the two interconnection lines. At the clocked element 10, PSK signals V_x and $V_{\bar{x}}$ are demodulated to recover the digital signal X and the clock signal.

Please amend paragraph number **[0035]** as follows:

[0035] Transistor amplifier circuit 29 is made up of diode-connected PMOS load transistor 35 and NMOS transistor 37. The demodulator circuit of FIG. 8 takes advantage of the nonlinear characteristics of PMOS load transistor 35 to recover digital data from PSK signals. For simplicity, it can be assumed that PMOS load transistor 35 and NMOS transistor 37 have matching characteristics. Power supply voltage V_{DD} is connected to the source of PMOS load transistor 35. Power supply voltage $V_{DD} = 4V_T$, where V_T is the threshold voltage of the PMOS load transistor 35 and NMOS transistor 37. The nominal DC voltage at the output of differential amplifier 27 and the input of transistor amplifier circuit 29 is $2V_T$ when no AC signal is output by differential amplifier 27. The corresponding voltage at the output of transistor amplifier circuit 29 is also $2V_T$. When V_x and $V_{\bar{x}}$ are applied to the inputs of differential amplifier 27, the output is:

$V_1 = 2V_T + 2A\cos(\omega t)\sin(\varphi)$ when X has a logical high value and $V_1 = 2V_T$ when X has a logical low value.

Please amend paragraph number **[0037]** as follows:

[0037] RC filter 31, which is a simple RC low pass filter at the output of transistor amplifier circuit 29, is made up of resistor 39 having a resistance R3 and capacitor ~~41having~~ 41 having a capacitance C3. The output of RC filter 31 is:

$V_3 = 2V_T - \frac{1}{2}[(4A^2/(4V_T))\sin^2(\varphi)]$,

which is the DC component of the output of transistor amplifier circuit 29 and corresponds to the average value of cosine squared. Signal V_3 is input to comparator 33 and compared to reference signal $V_{ref} = 2V_T$ to produce an output signal V_4 which has a value of either $\sin^2(\varphi)$ or zero. V_4 is the recovered digital data signal.